Internal Microwave Propagation and Distortion Characteristics of Travelling-Wave Amplifiers Studied by Electro-Optic Sampling

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Abstract

The internal signal propagation and saturation characteristics of two monolithic microwave travelling-wave amplifiers (TWA) are measured by electro-optic sampling. Gate and drainline responses are compared with theory and simulation, leading to revisions in the FET models. Drain voltage frequency dependence and harmonic current propagation together lead to more complex saturation behavior than is discussed in the literature.

Introduction

The frequency response and distortion characteristics of monolithic travelling-wave amplifiers (TWA) depend upon the propagation characteristics of microwave signals along the gate and drain transmission lines. The bandwidth and gain flatness of the amplifier are set by the finite cutoff frequencies of the periodically loaded lines, the line losses due to.FET input and output conductances, and the mismatch between gate and drain propagation velocities. The gain compression characteristics are set by several saturation mechanisms in the transistors, the power at which each mechanism occurs in each FET, and by the propagation of both the amplified signal and the generated distortion products. While some of these factors are considered in the modeling and design of a TWA, the model can be verified only by measurement of the amplifier's external scattering parameters; if an amplifier does not perform to expectations, the cause is not easily identified. If the voltages at the internal nodes of the amplifier could be measured, the amplifier's characteristics would be much better understood. Such measurements are now possible using electro-optical techniques.

We have developed a system for direct electro-optic sampling in GaAs integrated circuits [1-3]. In contrast to the external approach of Valdmanis, et al. [4], our system, which measures the electric-field-induced changes in polarization of pulses of sub-bandgap laser radiation as they pass through the GaAs substrate of the IC, can non-invasively measure the voltages at arbitrary points within the circuit. The sampler currently has a bandwidth of 70 GHz, a timing drift of 1 ps/minute, a measured noise floor of -60 dBm (1 Hz), and can be configured to emulate either a sampling oscilloscope or a network analyser. Using the sampler we have investigated the causes of bandlimiting and gain compression in two microwave TWA's.

Amplifiers Tested

In a distributed amplifier, a series of small transistors are connected at regular spacings between two high-impedance transmission lines. The high-impedance lines and the FET capacitances together form synthetic transmission lines, generally of 50 ohm characteristic impedance. Series stubs are used in the drain circuit, equalizing the phase velocities of the two lines and, at high frequencies, providing partial impedance matching of the drain output impedances and thus increasing the gain. By using small devices at small spacings, the cutoff frequencies due to the periodicities of the synthetic lines can be made larger than the bandwidth limitations associated with the line attenuations arising from FET gate and drain conductances; thus gain-bandwidth products approaching f_{max} can be attained [5]. The amplifiers studied are a 5-FET TWA for 2-18 GHz which uses microstrip transmission lines and a novel 5-FET TWA for 2-20 GHz designed with coplanar waveguide transmission lines (fig. 1) [6].

Small-Signal Measurements

By driving the TWA input with a swept-frequency sinusoid of small amplitude and then positioning the laser probe near the FET gate and drain terminals, we measure the small-signal transfer function from the input to each of these nodes, showing relative drive levels at the FET gates and output levels at the FET drains.

Packaging problems were found in testing the coplanar TWA; the amplifier chip, which showed 5.5 dB gain to 19 GHz, gave 5 dB gain to only 8 GHz when bonded to microstrip transmission lines. The long ground current path between the chip and the microstrip ground

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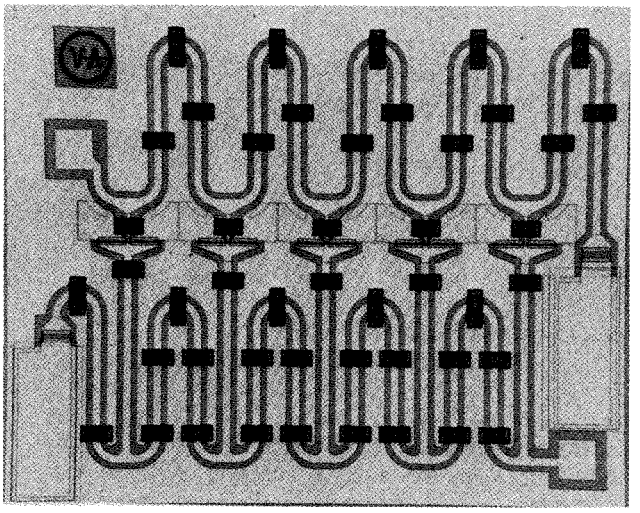

Figure 1: 2-20 GHz TWA using coplanar lines.

planes was suspected; optically probing the potential between the chip and package ground planes showed that the chip ground potential is only 5 dB below the input signal at high frequencies (fig. 2), indicating substantial package ground inductance. This inductance provides feedback and thus degrades gain. A package with coplanar waveguide transmission lines gave improved performance, but has not yet been optically probed.

The microstrip amplifier provides 6 dB gain to 18 GHz, while simulation predicts 7 dB gain to 20 GHz. The gate voltage curves for this amplifier (fig. 3) show several features: the rolloff beyond 18 GHz is the cutoff of the synthetic gate line, the slow rolloff with frequency at gates 3,4, and 5 is gate line attenuation, and the ripples are standing waves resulting from the gate line being misterminated. This data was compared to simulations using SuperCompact (TM); the simulator's optimizer was then used to adjust process-dependent circuit parameters to obtain the best fit to the measured data (fig. 4). Model gate termination resistance increased to 80 ohms , C_{gs} increased from 1.0 to 1.14 pF/mm, C_{gd} from 0.03 to 0.06 pF/mm, source resistance r_s increased from 0.58 to 0.72 ohms, and source inductance decreased from 0.14 to 0.10 nH; these values fall within normal process variations. Interference between the forward and reverse waves on the drain line results in strong frequency dependence of the drain voltages (fig. 5); this can be predicted by simple analysis.

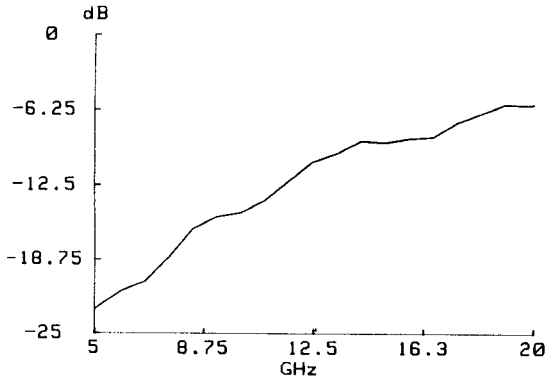

Figure 2: Chip ground potential relative to carrier potential, as a fraction of input voltageon the coplanar TWA.

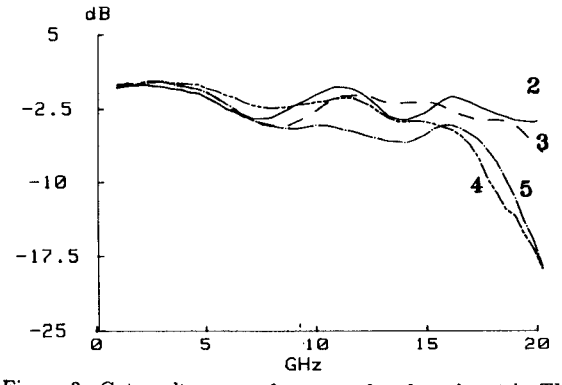

Figure 3: Gate voltage vs. frequency for the microstrip TWA; devices are numbered in order of propagation of forward wave.

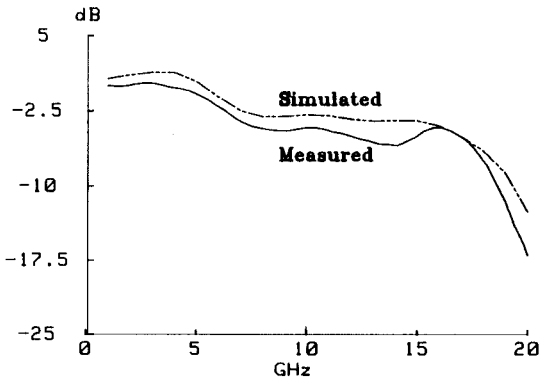

Figure 4: Comparison between simulated and measured gate 4 voltage after adjustment of the model to obtain best fit to measurements.

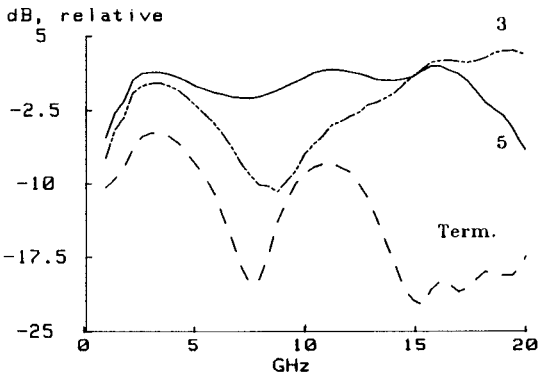

Figure 5: Measured voltage at drain 5, drain 3 and drain reverse termination of microstrip TWA.

Drain Voltage Distribution

After Ayasli [7], if the wavelength is much greater than the spacing between the FET's, the synthetic lines can be approximated as continuous structures coupled by a uniformly distributed transconductance. The lines then have characteristic impedances and phase velocities given by the sum of distributed and lumped capacitances and inductances per unit length [7]; the line impedances (Z_o) and velocities (V_p) are generally made equal. The lines then have propagation constants given by:

(1)

$$\gamma_g = \alpha_g + j\beta_g \simeq \frac{r_g \omega^2 C_{gs}^2 Z_o}{2l} + j\omega/V_p$$

(2)

$$\gamma_d = \alpha_d + j\beta_d \simeq \frac{Z_o G_{ds}}{2l} + j\omega/V_p$$

Where l is the FET spacing, C_{gs} is the gate-source capacitance, r_g is the gate resistance, G_{ds} is the drain-source conductance, and a forward propagating wave is of the form $e^{-\gamma z}$. The voltage along the drain line is

(3)

$$V_d(z) = \frac{Z_o g_m V_{in}}{2l} e^{-\gamma_g z} \left\{ \frac{1 - e^{(\gamma_g - \gamma_d)z}}{\gamma_d - \gamma_g} + \frac{1 - e^{(\gamma_g + \gamma_d)(z-nl)}}{\gamma_d + \gamma_g} \right\}$$

where n is the number of FET's, g_m is the FET transconductance, V_{in} is the input voltage, and z is the distance along the drain line, with the origin located at the drainline reverse termination. Ignoring line attenuation, (3) becomes:

$$\|V(z)\| = \frac{Z_o g_m V_{in}}{2l} \sqrt{z^2 + z\frac{sin(2\beta(nl-z))}{\beta} + \frac{sin^2(\beta(nl-z))}{\beta^2}}$$

(4)

which is plotted in figure 6. We see that the drain-line reverse termination does not absorb power at high frequencies. Furthermore, at high frequencies the input power is absorbed primarily in the FET input resistances and not in the gateline termination. Thus at high frequencies the TWA is a directional coupler with gain. The terminations serve to reduce the low-frequency power gain below the maximum available gain, but do not waste available gain near the cutoff frequency. The predicted frequency-dependent drain voltage distributions also complicate the large-signal operation of the amplifier.

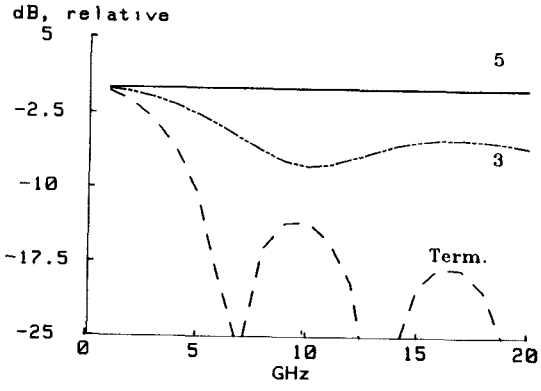

Figure 6: Voltage vs frequency at drain 5, drain 3 and drain reverse termination as calculated by eq. (4).

Saturation Mechanisms

The nonlinearities and power limitations in FET amplifiers include gate forward conduction, pinchoff, drain saturation, and drain breakdown. In a single FET amplifier, the loadline can be chosen so that all these limits are reached simultaneously, maximizing the output power before saturation. Ayasli [8] and Ladbrooke [9] extend this result to travelling-wave amplifiers by assuming that under appropriate design conditions (tapered gate and drain lines) the gate voltages and drain voltages of all FET's can be made equal, thus causing all devices to saturate simultaneously. However, as is shown by equation (3) and by figure 5, the reverse wave on the drain line complicates the problem; in the uniform drain line case, the drain voltages are equal only at low frequencies, and, by equation (3), the reverse wave introduces a phase shift between the gate and drain voltages of each FET. Thus, in the uniform drain line case, neither the conditions for simultaneous saturation of all FET's nor the conditions for simultaneously reaching all saturation mechanisms in a given FET can be met; similar conclusions may also apply for the tapered line case.

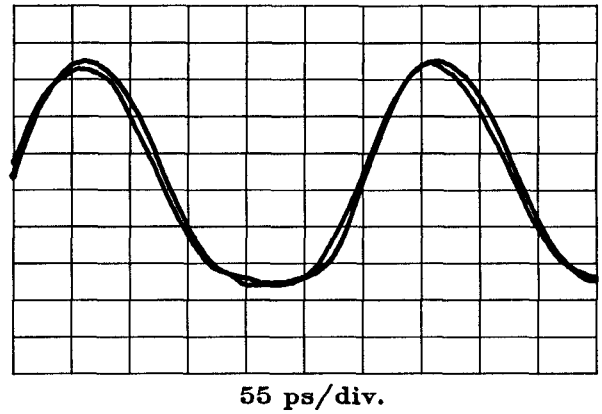

Figure 7: Saturation at drains 4 and 5 of microstrip TWA; 3 GHz, 7 dBm input power

The 2-18 GHz microstrip amplifier has 1 dB gain compression at 7 dBm input power, and is not optimized for maximum power output; the lines are not tapered and the bias is such that drain saturation occurs first. At 3 GHz, the small-signal voltages at the drains of the last three devices are approximately equal, thus clipping occurs simultaneously at these three devices (fig. 7).

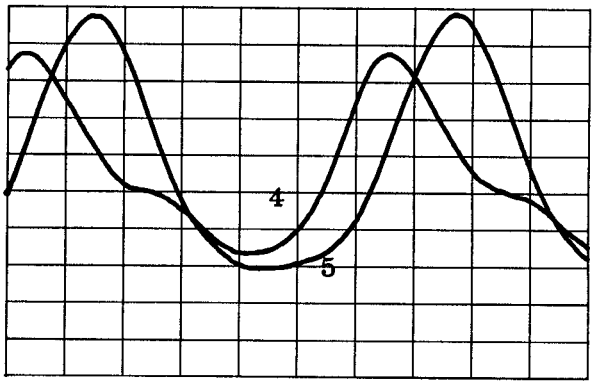

Figure 8: Saturation at drains 4 and 5 of microstrip TWA; 10 GHz, 7 dBm input power

At 10 GHz the distortion at the 1 dB compression point is complicated by phase shifts between the 10 GHz fundamental and the 20 GHz generated harmonic currents (fig. 8). The 10 GHz small-signal voltage at drain 5 is 1.5 dB larger than that at drain 4, thus FET 5 saturates more strongly. The 20 GHz harmonic current generated at FET 5 produces equal forward and reverse drain voltage waves at 20 GHz. With 10 ps line delay between drains 4 and 5, the 20 GHz reverse wave from FET 5 undergoes 20 ps relative phase delay (which is 72 degrees of a 10 GHz cycle) before combining with the the 10 GHz forward wave at drain 4. The resulting voltage waveform at drain 4 would then approximate a sawtooth function; drain saturation at FET 4 then clips the peak negative excursion. Depending upon the line delay between successive drains, the reverse-propagating harmonic currents can either increase or decrease the peak voltages at other drains, increasing or decreasing the saturation at prior devices.

At 18 GHz the small-signal drain voltage at drain 4 is larger than that at drain 5, thus FET 4 will saturate more strongly than will FET 5. The 36 GHz harmonic currents generated at drain 4 are beyond the cutoff frequency of the synthetic drain line; the generated 36 GHz forward wave thus experiences significant dispersion and attenuation relative to the 18 GHz forward wave, generating a slightly distorted but not clearly clipped waveform at drain 5.

Conclusions

We have studied the propagation of signals internal to microwave distributed amplifers with electro-optic sampling. Gate line attenuation and cutoff is observed, as is interference of the forward and reverse wave on the drain lines, both as predicted by theory. Using a microwave simulation program the circuit models can be adjusted to obtain a fit between simulated and measured internal node voltages, allowing detailed circuit diagnostics. Large-signal saturation characteristics of the amplifier are set by both the order of occurence of each saturation mechanism in each FET, and by the propagation of the generated harmonic currents through the circuit.

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